

Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 1 of 7

(503) 684-6200

Docket No.: 42390P6643C

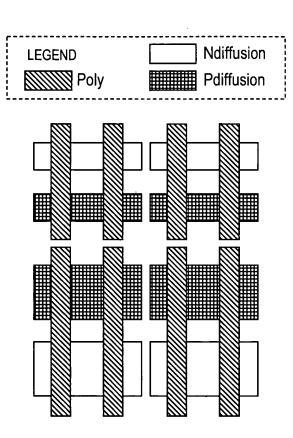


FIG. 1



Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 2 of 7

(503) 684-6200

Docket No.: 42390P6643C

Ndiffusion **LEGEND** Poly Pdiffusion

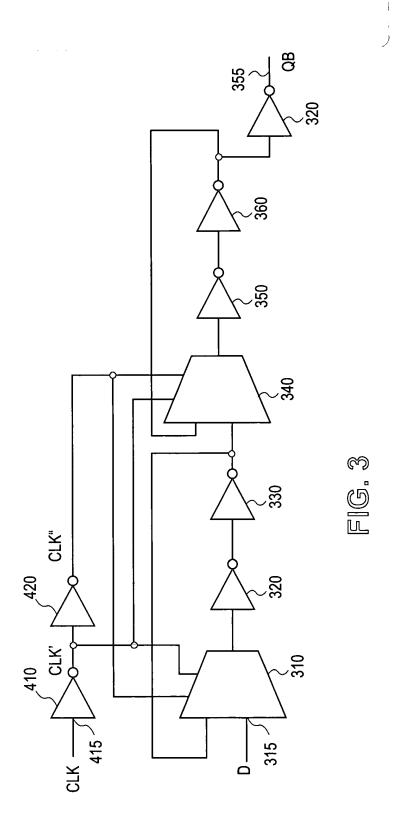
Traditional Approach

FIG. 2



Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 3 of 7

Docket No.: 42390P6643C





Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 4 of 7

(503) 684-6200

Docket No.: 42390P6643C

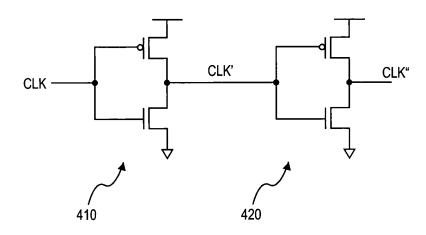
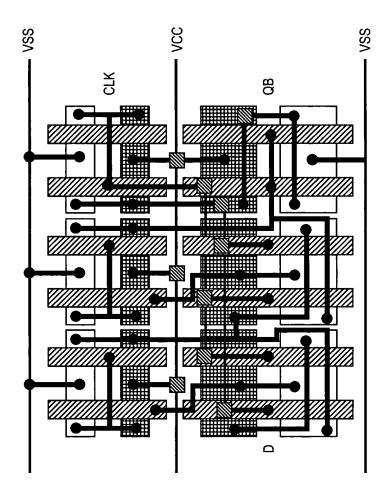


FIG. 4

Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 5 of 7

Docket No.: 42390P6643C



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Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 6 of 7

(503) 684-6200

Docket No.: 42390P6643C

Table 1

Name	Clock Pin Power	Notes
Capacitance Improved	0.06 pJ	FIG. 2
Si Arc	0.13 pJ	SiArc CBA
Traditional	0.15 pJ	FIG. 2

pJ = pico joules

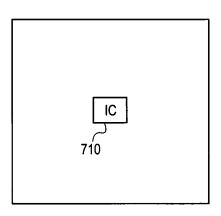
FIG. 6



Blakely, Sokoloff, Taylor & Zafman LLP Title: GATE ARRAY ARCHITECTURE 1st Named Inventor: Brian D. Possley Application No.: 09/902,912 Sheet: 7 of 7

(503) 684-6200

Docket No.: 42390P6643C



<u>700</u>

**FIG.** 7